PC05XT
TIME CODE GENERATOR MODULE

User's Guide

July 1994

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PC05XT TIME CODE GENERATOR MODULE

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CHAPTER 1
INTRODUCTION

1.0 GENERAL

This Operation and Technical Manual provides the following information on the PC05XT Time Code Generator:

- Functional Description, Specifications, and Definition of Terms
- Installation and Setup Details
- Operation and Software Interface Details
- I/O Signal Information
- Theory of Operation
- Programming Examples
- Drawing Set

1.1 FUNCTIONAL DESCRIPTION

The PC05XT Time Code Generator module is a modulated serial time code generator for use in a PC XT/AT computer environment. The principal performance specifications are listed in Section 1.2. The PC05XT module is shown in Figure 1-1. The PC05XT provides the following capabilities:

- Generates commonly used time code formats: IRIG A, IRIG B, IRIG G, 2137, XR3, and NASA 36.
- Precise time base stability (± 0.005 %).
- Generates time code in forward or reverse.
- Generates time code at six rates in addition to real time.
- Generates an embedded 30 character message for IRIG A, B.
- Provides a DC Level Shift output.
- Provides 1 PPS, 10 PPS, and 100 PPS outputs.
- Adjustable output amplitude and modulation ratio.
- Can operate with an external clock (1, 5, 10 MHz).
- Can synchronize to an external 1 PPS pulse.
- Drives Datum time display equipment.
- Optional plug-on modules provide synchronization to external time codes.

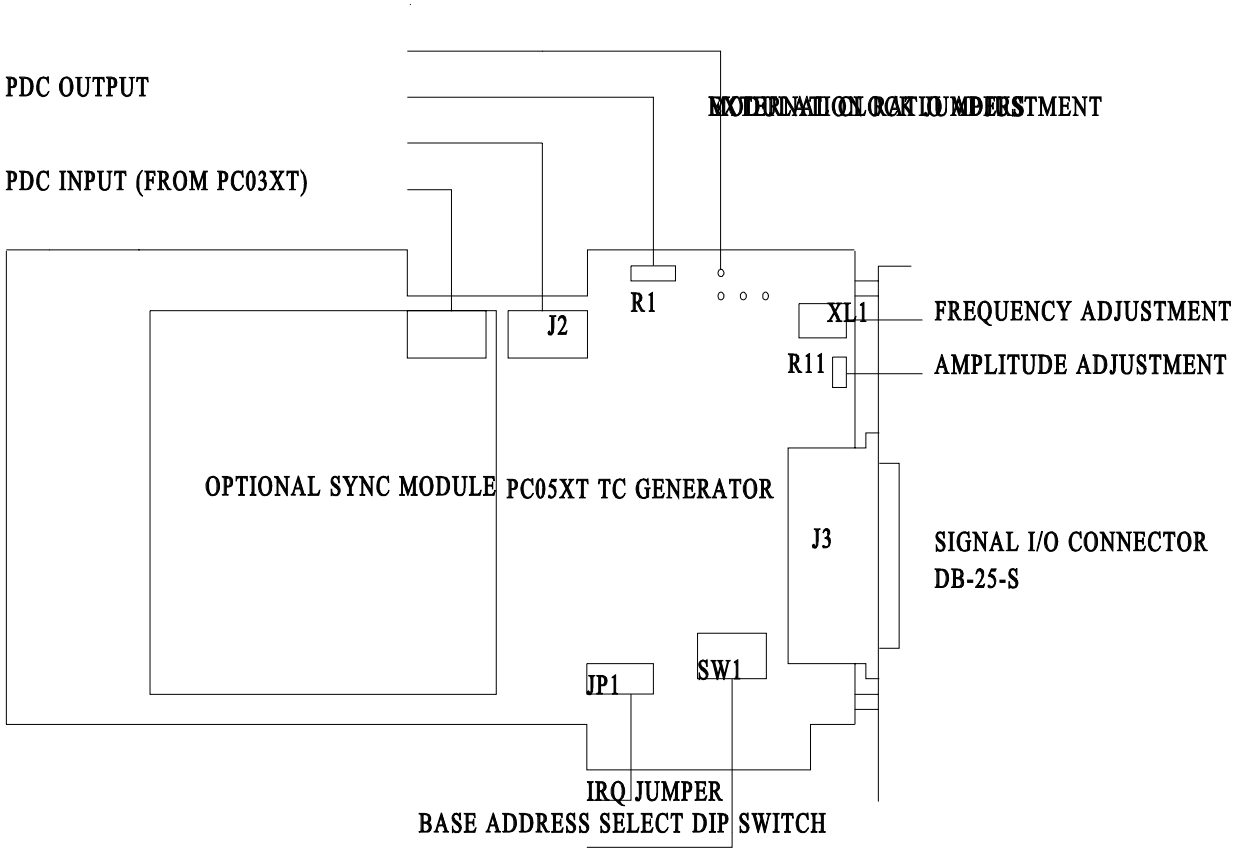

Figure 1-1: PC05XT Time Code Generator module

1.2 SPECIFICATIONS

Size:	Full length PC XT plug-in module.
Output Amplitude:	0 - 10 Vpp (unloaded) 0 - 5 Vpp (50 ohm load)
Modulation Ratio:	2:1 to 8:1
Time Code Formats:	IRIG A, IRIG B, IRIG G, 2137, XR3, NASA 36
Generating Rates:	1/8X, 1/4X, 1/2X, Real Time, 2X, 4X, 8X
Power Consumption:	+ 5 Vdc @ 700 mA +12 Vdc @ 50 mA - 12 Vdc @ 50 mA
Internal Time Base:	
Stability:	± 0.0005 % +20 ^{o}C to + 35 ^{o}C ± 0.0025 % 0 ^{o}C to + 70 ^{o}C
Accuracy:	± 0.0001 % +25 ^{o}C
Adjustment:	± 30 ppm

1.3 TIME CODE FORMATS

The widespread use of coded timing signals to assist in the correlation of intercept and test data began in the early 1950's. These signals can be decoded in real time to indicate the current Time of Day (TOD) or recorded along with intercept/test data on magnetic tape recorders for post processing and time correlation.

Hundreds of time code formats were developed - one for each agency involved. During the early 1960's the Inter-Range Instrumentation Group (IRIG) promoted a series of 'standard' time code formats now loosely referred to as 'IRIG Time Codes'. The PC05XT generates three of these formats:
IRIG A, IRIG B, and IRIG G.

Several other formats - XR3, 2137, and NASA 36 - are also generated by the PC05XT and still enjoy relatively widespread use within their originating agencies..

More complete details on these and other time code formats are available, free of charge, on request from either Bancomm Division or Datum Inc in the form of the Handbook of Time Code Formats. Figure 1-2 illustrates a frame of IRIG A, B or G time codes.

Figure 1-2: IRIG Time Code Format

1.4 DEFINITION OF TERMS

The terms used throughout this manual are defineed below.

1 PPS: 1 Pulse Per Second. A pulse whose low to high going edge occurs at the time code ON TIME.

CARRIER: The sinusoidal signal which when amplitude modulated with time code becomes a time code signal. (i.e. IRIG B uses a 1 kHz carrier).

FORWARD: Denotes the direction of time code where time increases.

ON TIME: The point in the time code frame where the encoded time is true.

REAL TIME RATE: The time code rate at which the time code data changes by 1 second for every 1 real time second.

REVERSE: Denotes the direction of time code where time decreases.

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CHAPTER 2
INSTALLATION AND SETUP

2.0 GENERAL

The PC05XT Time Code Generator module is a full length XT size board for use in an PC XT/AT computer. This chapter details the steps required to setup and install the PC05XT in the computer. This chapter also describes the installation of the option plug-on modules.

2.1 BASE ADDRESS SELECTION

The PCbus allocates 512 bytes of I/O port addresses for plug-in boards located at address 0x200 - 0x3FF. The PC05XT Generator uses a block of 16 I/O ports. Switch positions 1 - 5 of dip switch SW1 correspond to PCbus address bits A8 - A4 and are used to select the base address for the PC05XT. Switch positions 6 - 8 should be left in the ON (CLOSED) position. To select a base address, set each of the 5 dip switches to the ON (CLOSED) or OFF (OPEN) position as shown in Table 2-1. Setting a dip switch to the ON position selects a logical 0 for that address bit, and the OFF position selects a logical 1.

2.2 INTERRUPT JUMPER

The PCbus provides 6 active high interrupt lines for user interrupts (IRQ2 - IRQ7). Although some of these lines are generally dedicated to peripherals (disk drives, serial ports, etc), access to any one of the six lines is provided. The PC05XT can generate a PCbus interrupt when a status word is loaded into the Status Byte Register (see Chapter 3).

Jumper JP1 is used to select one of the six interrupt lines or to disconnect all interrupts for those applications that do not use interrupts. The Jumper positions (2 - 7) are shown in Figure 2-1. To disconnect the interrupts completely, place the jumper plug horizontally on the top row of JP1 or remove it from the board.

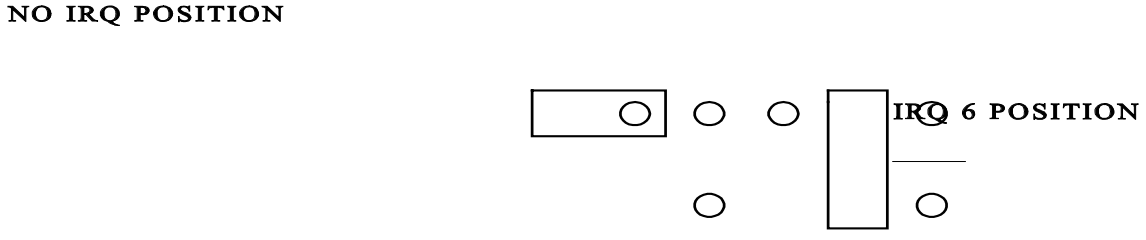

Figure 2-1: Jumper JP1 (Interrupt Request)

Table 2-1: PCbus Base Address Selection

PCbus I/O ADDRESS RANGE	SW1 DIP SWITCH				
	1	2	3	4	5
0200 - 020F	ON	ON	ON	ON	ON
0210 - 021F	OFF	ON	ON	ON	ON
0220 - 022F	ON	OFF	ON	ON	ON
0230 - 023F	OFF	OFF	ON	ON	ON
0240 - 024F	ON	ON	OFF	ON	ON
0250 - 025F	OFF	ON	OFF	ON	ON
0260 - 026F	ON	OFF	OFF	ON	ON
0270 - 027F	0FF	OFF	OFF	ON	ON
0280 - 028F	ON	ON	ON	OFF	ON
0290 - 029F	OFF	ON	ON	OFF	ON
02A0 - 02AF	ON	OFF	ON	OFF	ON
02B0 - 02BF	OFF	OFF	ON	OFF	ON
02C0 - 02CF	ON	ON	OFF	OFF	ON
02D0 - 02DF	OFF	ON	OFF	OFF	ON
02E0 - 02EF	ON	OFF	OFF	OFF	ON
02F0 - 02FF	OFF	OFF	OFF	OFF	ON
0300 - 030F	ON	ON	ON	ON	OFF
0310 - 031F	OFF	ON	ON	ON	OFF
0320 - 032F	ON	OFF	ON	ON	OFF
0330 - 033F	OFF	OFF	ON	ON	OFF
0340 - 034F	ON	ON	OFF	ON	OFF
0350 - 035F	OFF	ON	OFF	ON	OFF
0360 - 036F	ON	OFF	OFF	ON	OFF
0370 - 037F	OFF	OFF	OFF	ON	OFF
0380 - 038F	ON	ON	ON	OFF	OFF
0390 - 039F	OFF	ON	ON	OFF	OFF
03A0 - 03AF	ON	OFF	ON	OFF	OFF
03B0 - 03BF	OFF	OFF	ON	OFF	OFF
03C0 - 03CF	ON	ON	OFF	OFF	OFF
03D0 - 03DF	OFF	ON	OFF	OFF	OFF
03E0 - 03EF	ON	OFF	OFF	OFF	OFF
03F0 - 03FF	OFF	OFF	OFF	OFF	OFF

2.3 EXTERNAL TIME BASE SELECTION

To drive the PC05XT Generator with an external clock the board must be strapped (wire jumpered) for the desired input frequency. Table 2-2 shows the jumper for each input frequency. Do not install more than one jumper.

The external frequency input can be sinusoidal or TTL. The input is transformer coupled on the board, and the return line is normally left floating (not at GROUND). To ground the return line install a wire jumper from E1 to E2.

Table 2-2: External Clock Input Frequency Selection

FREQUENCY	JUMPER
1 MHz	E3 TO E6
5 MHz	E4 TO E7
10 MHz	E5 TO E8
Ground Return	E1 TO E2

2.4 PC05XT CHASSIS INSTALLATION

To install the PC05XT into a PC proceed as follows:

1) Remove the computer chassis cover.

2) Select a vacant expansion slot and remove the blank rear panel bracket. Save the screw.

3) Slide the PC05XT module straight down to engage the card edge guide at the front of the unit and the card edge connector at the bottom.

4) Fasten the top of the bracket to the chassis using the screw that was saved from Step 2.

5) Replace the chassis cover.

2.5 OPTIONAL PLUG-ON MODULE INSTALLATION

To install an optional plug-on module onto a PC05XT proceed as follows:

1) Remove the PC05XT from the PC chassis.

2) The PC05XT has two 20 Position terminal strips mounted on the board (J5, 6). These engage two mating socket strips on the plug-on module. Very carefully, plug the module onto the PC05XT so that the PDC connector is next ot the PC05XT's J2 PDC.

3) Return the PC05XT with plug-on module to the PC chassis.

4) If the sync module requires a PDC input then connect the plug-on module's PDC connector to the PC03XT PDC with a 20 position flat cable.

CHAPTER 3
OPERATION AND SOFTWARE INTERFACE

3.0 GENERAL

This chapter describes the operation and software interface for the PC05XT Time Code Generator module. Refer to Chapter 2 for installation and setup details. All data transfers between the PCbus and the PC05XT are byte wide I/O operations.

3.1 PCbus INTERFACE

The PC05XT uses a dual port RAM for communication between the PCbus and the PC05XT on-board microprocessor. One port is connected to the PCbus and the other port is connected to the PC05XT MPU. The PC05XT requires 64 bytes of control and status data. These 64 bytes are mapped into just 16 bytes of PCbus I/O address space. This mapping is achieved by dividing the 64 bytes into 4 blocks of 16 bytes. A block is selected by writing the block number (0,1,2,3) into the block select register which is always mapped at offset 0 (Base Address + 0). The block select register can be read to determine the currently selected block. The address of each control/status data byte is designated by an offset from the base address.

3.2 CONTROL AND STATUS DATA

This section describes the control and status data used for controlling the operation of the PC05XT. Section 3.3 provides the details on how to use the control and status data to achieve the desired functions. Table 3-1 summarizes the control and status data. Offset values and data are in hex notation. The asterisk (*) in the RESET column indicates the reset condition for that function.

3.2.1 BLOCK SELECT REGISTER (BLOCKS 0-3 OFFSET 0x0)

The block select register is mapped at offset 0 for all blocks. The block select data byte must have a value of 0, 1, 2, or 3, which corresponds to blocks 0, 1, 2, or 3. The block select register can be read to determine the currently selected block.

3.2.2 CONTROL Byte (BLOCK 0 OFFSET 0x1)

The Control byte controls a number of functions on the PC05XT. It controls the external 1 PPS synchronization capabilities, optional plug-on synchronization modules, generator output, 30 character message. It also provides a means of resetting the on board microprocessor. After writing to the Control byte, the user must write the 'Process Control Byte' command to the Command byte.

Table 3-1: PC05XT Control and Status Data

BLOCK 0			
OFFSET (HEX)	**DATA**	**RESET**	**DESCRIPTION**
0x1			**CONTROL Byte**
	00	*	Disable External 1 PPS Sync
	01		Enable Continuous Ext 1 PPS Sync
	02		Enable One Ext 1 PPS Sync
	03	*	Disable Ext Time Code Sync
	04		Enable Ext Time Code Sync
	05		Disable Generator Output
	06	*	Enable Generator Output
	07	*	Disable 30 Character Message
	08		Enable 30 Character Message
	09	*	Reset Microprocessor
	0A	*	Select PDC 1 PPS for Real Time Sync
	0B		Select J3 1 PPS for Real Time Sync
	0C	*	Disable PDC Time Data for RT Sync
	0D		Enable PDC time Data for RT Sync
0x2			**TIME CODE FORMAT Byte**
			Generated Time Code Format
	X0		IRIG B
	X1		IRIG A
	X2		IRIG G
	X3		2137
	X4		XR3
	X5		NASA 36
			Synchronizing Time Code Format
	0X	*	IRIG B
	1X		IRIG A
	2X		IRIG G
	3X		2137
	4X		XR3
	5X		NASA 36

Table 3-1: PC05V Control and Status Data (continued)

BLOCK 0			
OFFSET (HEX)	**DATA**	**RESET**	**DESCRIPTION**
0x3			**RATE/DIRECTION Byte**
	00		1/8 Forward
	01		1/4 Forward
	02		1/2 Forward
	03	*	Real Time Forward
	04		2X Forward
	05		4X Forward
	06		8X Forward
	10		1/8 Reverse
	11		1/4 Reverse
	12		1/2 Reverse
	13		Real Time Reverse
	14		2X Reverse
	15		4X Reverse
	16		8X Reverse
0x4 - 0xC			**PRESET TIME Bytes**
0x4	0-9	0	Days Hundreds
0x5	0-9	0	Days Tens
0x6	0-9	0	Days Units
0x7	0-2	0	Hours Tens
0x8	0-9	0	Hours Units
0x9	0-5	0	Minutes Tens
0xA	0-9	0	Minutes Units
0xB	0-5	0	Seconds Tens
0xC	0-9	0	Seconds Units
0xD			**CHECKSUM BYTE**

Table 3-1: PC05V Control and Status Data (continued)

BLOCK 0			
OFFSET (HEX)	**DATA**	**RESET**	**DESCRIPTION**
0xE			**STATUS Byte (Generates PCbus IRQ)**
	00	*	Checksum Valid
	01		Preset Time Loaded
	02		Synchronized to Ext 1PPS
	03		Invalid Command Byte
	04		Invalid Time Code Format
	05		Invalid Rate
	06		Invalid Direction
	07		Invalid Preset Time
	08		Invalid Control Byte
	09		Generator Output Disabled
	0A		Generator Output Enabled
	0B		External Time Code Sync Disabled
	0C		External Time Code Sync Enabled
	0D		Sync Time Code Format Loaded
	0E		Generator Output Time Loaded
0xF			**COMMAND Byte**
	00		Process All Control Data
	01		Process Control Byte
	02		Process Time Code Format Byte
	03	*	Process Rate/Direction Byte
	04		Load Preset Time Bytes
	05		Load 30 Character Message Bytes
	06		Load Sync Time Code Format Byte
	07		Output Current Generator Time

Table 3-1: PC05V Control and Status Data (continued)

BLOCK 1			
OFFSET (HEX)	**DATA**	**RESET**	**DESCRIPTION**
0x1 - 0xB			**GENERATOR OUTPUT TIME Bytes (ASCII)**
0x1		0	Days Hundreds
0x2		0	Days Tens
0x3		0	Days Units
0x4		0	Hours Tens
0x5		0	Hours Units
0x6		0	Minutes Tens
0x7		0	Minutes Units
0x8		0	Seconds Tens
0x9		0	Seconds Units
0xA		0	Seconds Tenths (IRIG A & IRIG G)
0xB		0	Seconds Hundredths (IRIG G)
0xC - 0xF		0	Not used
BLOCK 2			
OFFSET (HEX)	**DATA**	**RESET**	**DESCRIPTION**
0x1 - 0xF		0	**MESSAGE Bytes 1 - 15**
BLOCK 3			
OFFSET (HEX)	**DATA**	**RESET**	**DESCRIPTION**
0x1 - 0xF		0	**MESSAGE Bytes 16 - 30**

3.2.3 TIME CODE FORMAT Byte (BLOCK 0 OFFSET 0x2)

The Time Code Format byte determines which time code format the PC05XT will generate and which format will be used for synchronization purposes when using one of the optional plug-on modules. The lower nibble (4 bits) determines the generated time code format. The upper nibble determines the time code format of the input synchronizing time code (applicable only when using an optional plug-on sync module). After writing to the Time Code Format byte, the user must write the 'Process Time Code Format Byte' or 'Load Sync Time Code Format Byte' command to the Command byte.

3.2.4 RATE/DIRECTION Byte (BLOCK 0 OFFSET 0x3)

The Rate/Direction byte controls the rate and direction of the generated code. The PC05XT is unique in its ability to generate time code at rates other than real time and to generate time code in the reverse direction. The Rate/Direction byte is usually set to generate code at the real time rate in the forward direction.

Generating time code at non-real time rates (and in reverse) is useful for simulating the time code output from a tape recorder which can playback time code faster or slower than real time. Non-real time rates are also useful for exercising equipment and systems which operate on time code (time code translators, etc).

3.2.5 PRESET TIME Bytes (BLOCK 0 OFFSET 0x4 - 0xC)

The Preset Time bytes are used to load the generator with a preset time. The PC05XT will begin generating time code starting with the preset time after the 'Load Preset Time' command is sent. Nine bytes are used for the preset time (days hundreds to seconds units) and may be written in an ASCII or BCD format. The PC05XT ignores the upper 4 bits of each preset time digit.

3.2.6 CHECKSUM Byte (BLOCK 0 OFFSET 0xD)

The Checksum byte contains the 8 bit checksum from the firmware EPROM on the PC05XT. The checksum is calculated following power on or following a 'Reset MPU' command.

3.2.7 STATUS Byte (BLOCK 0 OFFSET 0xE)

The Status byte is used to report the result of a command to the user. For example, when the PC05XT is commanded to load a new preset time, the Status byte is used to let the user know that the new preset time has been loaded. When the PC05XT writes a new Status byte an interrupt is generated on the PCbus (if the interrupt jumper JP1 is installed). This PCbus interrupt is cleared by reading the Status byte.

3.2.8 COMMAND Byte (BLOCK 0 OFFSET 0xF)

The Command byte is used to tell the PC05XT to perform some action or to process some new data (e.g. preset time). For example, after loading the Preset Time bytes with a preset time, the user must write the value 4 to the Command byte which tells the PC05XT to start generating time code starting with the preset time. A change to the operating mode of the generator is a two step process. First, the user must write the appropriate control or status data byte(s) to the RAM. Second, the user must write the appropriate Control byte value to the Control byte (BLOCK 0 OFFSET 0xF) to signal the PC05XT to take action.

3.2.9 GENERATOR TIME OUTPUT Bytes (BLOCK 1 OFFSET 0x1 - 0xB)

The Generator Time Output bytes are loaded by the PC05XT in response to the 'Output Current Generator Time' command. The data (one byte per digit) is in an ASCII format. The time output has a resolution down to seconds for all time code formats and contains subsecond time for IRIG A (tenths of seconds) and IRIG G (tenths and hundredths of seconds). After the 'Output Current Generator Time' command is issued, the user should read the status byte until the 'Preset Time Loaded' status is read so that the user knows that the Generator Output Time bytes are valid.

3.2.10 MESSAGE Bytes (BLOCK 2-3 OFFSET 0x1 - 0xF)

The PC05XT has the ability to embed a 30 character message into the control character fields of the IRIG A and IRIG B time code formats. This 30 character message can be read by Datum time code reader modules. Block 2 is used to load the first 15 characters of the message and block 3 is used to load the last 15 characters. The individual message characters can be any 8 bit value desired. After loading the desired message bytes, the user must issue the 'Load Message' command. The message still needs to be enabled using the 'Enable Message' command.

3.3 FUNCTIONAL DESCRIPTION

Section 3.2 provided an overview of the PC05XT control and status data. This section describes how this data is used to achieve the desired functions. This section also provides the function description of the optional plug-on synchronizing modules.

3.3.1 PC05XT Initialization

Table 3-1 shows the reset state of the PC05XT. The easiest way for the user to initialize the PC05XT for time code format, preset time, etc. is to load all control and data bytes with the appropriate values and then to issue the 'Process All Control Bytes' command. Alternatively, the user may set up each function individually.

3.3.2 External 1 PPS Synchronization

The PC05XT provides a means of synchronizing its ON TIME mark to the rising edge of an external 1 PPS signal. The PC05XT provides three modes for synchronizing the generated time code to an external 1 PPS signal. In the first mode, the 1 PPS synchronization is completely disabled. In the second mode, the PC05XT is continuously synchronized to the external 1 PPS signal. In the final mode, the PC05XT synchronize to one external 1 PPS pulse and then automatically disable the external 1 PPS sync option.

When the third option (Enable One Ext 1 PPS Sync) is used, the generator will write the status byte (Synchronized to Ext 1 PPS) to the Status Byte register after it detects the 1 PPS signal.

Synchronizing the PC05XT to an external 1 PPS signal can produce a glitch in the time code signal near the ON TIME mark due to frequency offsets between the PC05XT's internal clock source and the time base used to produce the external 1P PS signal. This can be avoided by supplying an external clock input that is synchronous with the 1 PPS signal. See Section 3.3.3.

3.3.3 External Clock Input

The PC05XT uses an on board 10 MHz crystal oscillator with a stability of ± 0.0005 %. This oscillator provides an accuracy adjustment of ± 30 ppm. If you require a more precise time base, you may provide an external clock (sinusoidal or TTL) to the PC05XT. The external frequency must be either 1, 5, or 10 MHz. To use an external clock the user must install the appropriate jumper for the frequency being used (Refer to Section 2.3, "External Time Base Selection" for jumper installation). The PC05XT will then use the external frequency whenever the clock is present. If the external clock is removed, the PC05XT will automatically revert to its internal oscillator.

3.3.4 Time Code Amplitude/Ratio Adjustment

The amplitude of the time code output signal is adjustable from 0 to 10 Vpp (no load) or 0 to 5 Vpp (50 ohm load). The amplitude adjustment pot (R11) is accessible through the rear bracket and is labeled 'ADJ AMPL'. The modulation ratio (ratio of high amplitude to low amplitude cycles) is adjustable from 2:1 to 8:1. The modulation ratio adjustment pot (R1) is accessible from the top of the module. The modulation ratio should normally be set to 3:1. The amplitude should normally be 2 - 3Vpp.

3.3.5 Internal Clock Adjustment

The PC05XT uses a very stable (± 0.0005 %) 10 MHz crystal oscillator for its time base. This oscillator has a frequency adjustment which is accessible from the rear bracket and is labeled 'FREQ'. The adjustment provides for a frequency offset of ± 30 ppm.

3.3.6 Optional Plug-On Synchronization Modules

The PC05XT can be equipped with an optional plug-on modules which provide synchronization to an external time code source. This allows for synchronization over a wide range of applications. Refer to Section 2.5, "Optional Plug-On Module Installation" for installation of the plug-on module.

The Tape Sync Module (-TS option): Is used to synchronize the PC05XT to a time code signal being decoded by a PC03XT Time Code Reader module operating on the same PCbus. With this option, the PC05XT can be synchronized to time codes running at non real time rates and in forward and reverse. The Tape Sync module provides synchronization to within approximately 200 µs by using a VCO circuit. This option is useful for synchronizing to a time code signal that has been reproduced from an magnetic tape recorder. This module can flywheel through short tape dropouts (i.e. short loss of time code signal). If the synchronizing code is lost, the PC05XT will experience a disruption in its output signal for approximately 1 - 3 seconds and will then continue to generate a proper time code signal.

The Tape Sync Option is controlled by the Enable/Disable External Time Code Sync commands (BLOCK 0 BYTE 0x1). When this option is enabled the PC05XT will sync its ON TIME mark to that of the sync code and will also generate the same time as the sync code.

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CHAPTER 4
I/O CONNECTORS

4.0 GENERAL

All PC05XT Generator I/O signals (except PDC) are available on the rear bracket connector J3. The J3 connector is a 15 pin DS type connector. Figure 1-1 shows the location of all connectors.

4.1 J3 SIGNAL I/O CONNECTOR

All I/O signals (except the PDC signals) are connected to the rear bracket 15 pin 'DS' connector. Table 4-1 shows the pin assignments for the J3 connector. These signals are described below.

- External 1 PPS Input: TTL input used to synchronize the generator ON TIME mark to an external 1 PPS signal.
- Frame Sync Output: TTL signal whose low to high going edge occurs once per time code frame and occurs ON TIME.
- Each Cycle Output: TTL representation of the time code carrier which is high during positive half cycles, low during negative half cycles.
- 1 PPS Output: 1 Pulse Per Second TTL output.
- 10 PPS Output: 10 Pulses Per Second TTL output.
- 100 PPS Output: 100 Pulses Per Second TTL output.
- Time Code Output: Modulated time code signal output.
- External Clock Input: 1, 5, or 10 MHz signal (sinusoidal or TTL) optionally used to drive the generator.
- External Clock Return: The external clock input is transformer coupled. If jumper E1 to E2 is installed then this signal is grounded.
- DC Level Shift: TTL output time code signal without the carrier.

Table 4-1: J3 I/O Connector Pin Assignments

J3 PIN	SIGNAL DESCRIPTION
1	External 1 PPS Input
2	Ground
3	Frame Sync Output
4	Each Cycle Output
5	10 PPS Output
6	Ground
7	100 PPS Output
8	Ground
9	Time Code Output (Modulated)
10	Ground
11	External Clock Input
12	External Clock Return
13	1 PPS Output
14	Ground
15	DC Level Shift Output (Unmodulated)

4.2 J2 PDC CONNECTOR

The J2 20 pin connector carries the PDC signals which can be used to drive the M80D-LU time display module. Table 4-2 lists, the pin assignments for the J2 connector.

The signals carried on the PDC (Peripheral Data Connector) are generally used to drive other Datum products which require decoded time such as the M80D-LU display module. The signals can, however, be used by the user for a variety of applications.

Decoded time is transmitted over the PDC once per second using the PDC ENABLE* and D0 - D7 lines in a byte serial fashion (i.e. a burst of 9 bytes are sent) just after the 1 PPS mark. Table 4-3 gives the D0 - D7 encoding. The lower nibble contains the BCD encoded time digit, and the upper nibble determines which digit has been transmitted. The D0 - D7 data lines are valid when PDC ENABLE* is low.

EACH CYCLE is a TTL representation of the time code carrier (high during positive half cycles, low during negative half cycles). 1 PPS is a TTL signal, 1 carrier cycle wide, whose rising edge occurs on time. FRAME SYNC is a TTL signal, 1 carrier cycle wide, whose rising edge occurs once per frame at the on time mark.

Table 4-2: PDC Pin Assignments

PDC	SIGNAL DESCRIPTION	PDC	SIGNAL DESCRIPTION
1	Ground	2	PDC ENABLE*
3	D0	4	D1
5	D2	6	D3
7	D4	8	D5
9	D6	10	D7
11	EACH CYCLE	12	Not used
13	1 PPS	14	Not used
15	Not used	16	Not used
17	FRAME SYNC	18	Ground
19	+ 5 Vdc	20	+ 5 Vdc

Table 4-3: PDC Data Format

D7	D6	D5	D4	D3 - D0 (BCD)
0	0	0	0	Days Hundreds
0	0	0	1	Days Tens
0	0	1	0	Days Units
0	0	1	1	Hours Tens
0	1	0	0	Hours Units
0	1	0	1	Minutes Tens
0	1	1	0	Minutes Units
0	1	1	1	Seconds Tens
1	0	0	0	Seconds Units

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CHAPTER 5
THEORY OF OPERATION

5.0 GENERAL

The PC05XT uses a Z80 microprocessor and support circuitry to digitally synthesize a modulated sine wave time code signal. Extensive use of Programmable Logic Devices (PLD) is made to reduce circuit area. The following sections describe the various functional areas of the PC05XT module.

5.1 INTERNAL/EXTERNAL TIME BASE PROCESSING

The internal time base supplied with the PC05XT will be one of two types of hybrid DIP oscillator. The optional type is more precise and the offset from center frequency can be adjusted through the rear panel. The 10 MHz signal from this timebase is divided down to 1 MHz which then goes to the programmable array logic (PAL) chip in U8.

The external time base, if used, is supplied through J3 to transformer T1 for isolation. It then triggers a biased Schmitt trigger and is divided appropriately down to 1 MHz and is presented to the PAL U8. One-shot U26, which is configured as an activity sensor for the external frequency input, also signals PAL chip U8 when a frequency is present.

PAL U8 selects the external frequency, if present, or the internal frequency, and supplies it to the divide-by-10 circuit which then goes to the reference side of the comparator U17. This comparator drives a voltage controlled oscillator U1 through some analog circuits. This phase-locked loop is intended to operate at 6.4 MHz, which is the frequency used to generate the time code.

5.2 SINEWAVE GENERATOR AND OUTPUT CIRCUITS

The 6.4 MHz described above is divided down through two synchronous counters, U2 and U6, that drive the inputs to the multiplexer U11 which is under firmware control. The output of the multiplexer is called SAMPLE. This signal, after being conditioned by PAL U22, is the clock that drives the FIFO to generate the sinewave carrier signal that the time code modulates. Digital to Analog Converter U15 receives the FIFO output through a latch U23 and outputs a differential signal which is amplified and buffered before being output on J3.

The FIFO resets itself through the ninth bit going hign and setting the flip-flop U9 which lowers the retransmit line for one half of a 6.4 MHz clock period.

5.3 TIME CODE TABLE AND SYNCHRONOUS CLOCKING

The most significant bit of the FIFO conveniently changes state as the sine wave crosses over 0 Volts, and this term is used by PAL U22 to derive several signals for use by other parts of the generator. ECOUT is the square wave representation of the output sinewave, which is output on the PDC (J2) and rear panel, and used to derive other signals. ECENA is a signal that goes high before the rising edge of ECOUT and lasts for one rising edge of the 6.4 MHz clock.

ECENA enables the clocking of the synchronous counters, U19, U20, and U21 that address the dual port code table RAM, U28. This dual port RAM contains two 1000-byte buffers which are loaded by software through one port and addressed by hardware through the other port for code generation.

The synchronous counters are also synchronously reset through the PAL U13. A bit set on D3 in the code table enables a reset, CTRS, for one rising edge of the 6.4 MHz clock, which also flips the address line A10 on the hardware side of the code table RAM through PAL U22, which determines the active buffer. The code table output D0 is the time code modulation envelope that is used to modulate the digital-to-analog converter U15 at Pin 14. It is also buffered and outputted from both the PDC and rear panel 'D' connector as the DC Level Shift signal.

5.4 EXTERNAL 1 PPS SYNCHRONIZATION

External 1 PPS synchronization is accomplished through PALs U8, PAL U13, PAL U22, and the input circuit through U24. Once the external 1 PPS is enabled, the synchronization will not occur until a rising edge after the event signal is low. When this rising edge occurs, it is latched and synchronized using the 6.4 MHz clock. This event then resets the FIFO to start the sinewave over, and resets the address counters for the code table. This will disrupt the present frame of code, but once the generator is synchronized, the new frame is in sync with the external event.

5.5 SYNCHRONIZATION OPTIONS INTERFACE

The PC05XT contains two 20 position terminal strips that allow an optional daughter board to be attached which are located at J5 and J6. These two connector strips contain address, data, and interrupt lines for software interfacing, and clock terms, enables, and sync terms to perform hardware functions. Identifier signals DT0 and DT1 allow the microprocessor to automatically enable the proper functions when a daughter board is installed. The PAL U8 routes the correct clocks and resets for use by the generator when a daughter board is performing a sync function.

5.6 DUAL PORT RAM COMMUNICATIONS PORT

As described in Chapter 3, communications are carried on through a dual port RAM, U35. Four blocks of 16 bytes are set aside for the transfer of information. The host system has access to only one block of 16 bytes at a time which is selected by writing the block number to the first byte at address 0. This data is latched in PAL U32 which controls the host side address lines A4, A5, and A6. When a byte is written to the top register of block 0, an interrupt is written to the CTC chip U37.

When the PC05XT communicates to the host, it writes to one address from the top of the RAM which generates an interrupt that is inverted in the PAL U32, and jumpered across JP1 if used. The host system then clears this interrupt by reading this status byte.

The base address is selected by comparing host address lines A4 through A8 with the programing switches SW1 and A9 to "1" in the comparator U33. When equality is reached, the RAM and address latches are enabled.

5.7 FIRMWARE OPERATIONS

The primary function of the firmware in the PC05XT is to keep the code table updated, which is an interrupt driven task. The main part of the program does some background tasks such as checking for update flags, and monitoring status for automatic functions.

Upon power up, the program calculates a check sum of the data in the EPROM, which is written to the communication port. It then proceeds to load all the variables with known initialization values and performs other functions that enable the microprocessor and support circuitry to operate properly.

The next step is to go into a programing mode with the default values stored in the EPROM. First, the output is disabled, then the sample rate is programed, the sine table in the FIFO is loaded, the code table is initialized with the current code, and then the code output is enabled.

As the code is being generated, the processor sets a flag at the end of frame interrupt, which results in the time being updated and loaded into the inactive buffer in the code table.

If the communication port is activated, another interrupt signals the microprocessor for service. If it instructs the system to load a new code type, or change direction and/or the rate, the generator again goes into the programing mode and the new values are loaded. If other instructions are given, they are carried out accordingly.

The system is automatically monitoring the status of the daughter board if installed. When this circuit is activated, the system enables it to sync the generator. If it becomes inactive, then the sync option board is disabled, and the system goes back to generating without synchronization.

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CHAPTER 6
PROGRAMMING EXAMPLES

6.0 GENERAL

This section provides programming examples which illustrate the software interface to the PC05XT Generator module. Examples are shown in a simple pseudo-code. The following two functions are used to indicate PCbus byte wide I/O reads and writes.

```
InPort(Offset)       /* returns data at specified address */
OutPort(Data,Offset) /* writes Data to specified address  */
```

6.1 TIME CODE FORMAT SELECTION

This example shows how to select the Generated Time Code Format (IRIG A in this example). Since no optional sync module is used, the Sync Time Code Format is not relevant.

```
OutPort(Ox0,0x0)  /* Select Block 0 */
OutPort(0x1,0x2)  /* Time Code Format = IRIG A */
OutPort(0x2,0xF)  /* Process Time Code Format Byte command */
```

6.2 PRESET GENERATOR TIME

This example shows how to preset a generator time. The time will be preset to 123 11:22:33.

```
OutPort(0x0,0x0)  /* Select Block 0 */
OutPort(0x1,0x4)  /* Days Hundreds digit */
OutPort(0x2,0x5)  /* Days Tens digit */
   .
   .
OutPort(0x3,0xC)  /* Seconds Units digit */
OutPort(0x4,0xF)  /* Load Preset Time Bytes command */
```

6.3 READ CURRENT GENERATOR TIME

This example shows how to read the currently generated time.

```
OutPort(0x0,0x0)  /* Select Block 0 */
OutPort(0x7,0xF)  /* Output Current Generator Time command */
While(InPort(0xE) != 0xE) Do Nothing  /* Wait for status */
OutPort(0x1,0x0)  /* Select Block 1 */
DH = InPort(0x1) /* Read days hundreds digit */
DT = InPort(0x2) /* Read days tens digit */
   .
   .
SU = InPort(0x9) /* Read seconds units digit */
```

6.4 ENABLE CONTINUOUS EXTERNAL 1PPS SYNC

This example shows how to enable the PC05XT to continuously synchronize to an external 1PPS signal using the on board sync circuitry (not the option RT sync module).

```
OutPort(0x0,0x0)  /* Select Block 0 */
OutPort(0x1,0x1)  /* Enable Continuous Ext 1PPS Sync */
OutPort(0x1,0xF)  /* Process Control Byte command */
```

6.5 RESET PC05XT MICROPROCESSOR

This example shows how to reset the PC05XT microprocessor which will return the module to its power on state.

```
OutPort(0x0,0x0)  /* Select Block 0 */
OutPort(0x9,0x1)  /* Reset MPU */
OutPort(0x1,0xF)  /* Process Control Byte command */
```

6.6 SYNCHRONIZE TO EXTERNAL IRIG A SIGNAL

This example shows how to sync the PC05XT to an external IRIG A time code signal with the optional Tape Sync Module (-TS option).

```
OutPort(0x0,0x0)  /* Select Block 0 */
OutPort(0x10,0x2) /* Sync to IRIG A */
OutPort(0x6,0xF)  /* Load Sync Time Code Format Byte */
OutPort(0x4,0x1)  /* Enable Ext Time Code Sync */
OutPort(0x1,0xF)  /* Process Control Byte command */
```

CHAPTER 7
DRAWING SET

7.0 GENERAL

This chapter contains the following schematic diagrams and assembly drawings with parts lists for the PC05XT Time Code Generator module.

- Schematic Diagrams, PC05XT TC Generator, Drawing No. 11290
- Assembly Diagrams, PC05XT TC Generator, Drawing No. 11293

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